# Allpass-Based Design, Multiplierless Realization and Implementation of IIR Wavelet Filter Banks with Approximate Linear Phase

#### Jassim M. Abdul-Jabbar

Department of Computer Engineering, College of Engineering, University of Mosul, Mosul, Iraq. drjssm@yahoo.com

#### Rasha Waleed Hmad

Department of Electrical Engineering, College of Engineering, University of Mosul, Mosul, Iraq. Rasha-Waleed87@yahoo.com

#### **Abstract**

In this paper, Bireciprocal Lattice Wave Digital Filters (BLWDFs) are utilized in an approximate linear phase design of 9<sup>th</sup> order IIR wavelet filter banks (FBs). Each of the two branches in the structure of the BLWDF realizes an Allpass filter. The low-coefficient sensitivity, excellent dynamic range and good stability properties of such filters allow their realization with short coefficient word lengths. Suitable coefficient wordlength representations are estimated for the best selection of some prescribed performance measures. The quantized coefficients are then realized in a multiplier less manner and implemented on Xilinx FPGA device. Therefore, less-complex infinite impulse response (IIR) wavelet filter bank structures are obtained with linear phase processing.

Keywords: AllPass Sections, Bireciprocal Lattice Wave Filters (BLWDFs), Linear Phase Processing, Quadrature Mirror Filters (QMFs), IIR Wavelet Filter Banks, FPGA Implementations.

## IIR التصميم بإعتماد الإمرارالكلي والتحقيق بدون مضارب لأجراف مرشحات مويجية نوع وبطور خطي تقريبي

رشا وليد حمد قسم الهندسة الكهربانية - كلية الهندس جامعة الموصل- الموصل-العراق Rasha-Waleed87@yahoo.com د. جاسم محمد عبد الجبار قسم هندسة الحاسوب- كلية الهندسة جامعة الموصل- الموصل-العراق drjssm@yahoo.com

#### الخلاصة

في هذا البحث، تم إستعمال المرشحات الرقمية الموجية من النوع المتشابك ثنائي التبادل في تصميم أجراف مرشحات مويجية من المرتبة التاسعة وبطور خطي تقريبي أن كلّ من الفرعين في هيكل تلك المرشحات الرقمية الموجية هو عبارة عن مرشح إمرار كلي. إن خواص هذه المرشحات المتمثلة بحسّاسية المعاملات المنخفضة والمدى الديناميكي الجيد والإستقرارية الجيدة تسمح بتحقيقها بمعاملات ذوات أطوال كلمات قصيرة. لقد تم تخمين الأطوال المناسبة لكلمات المعاملات لأفضل إختيار لبعض مقاييس الأداء الموصوفة مسبقاً إنّ المعاملات المكممة تمّ تحقيقها بعد ذلك بدون مضارب ومن ثم بنائها باستخدام أداة لشريحة FPGA نوع Spartan-3E وعليه فإن هياكل أجراف مرشحات مويجية نوع IIR أقل تعقيداً قد تم الحصول عليها وبمعالجة خطية الطور.

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#### I. Introduction

Discrete wavelets transform are often used in signal and image analysis and processing [1]. FIR wavelets filter banks (such as Daubechies and Haar filters) are commonly utilized in the design and realization of wavelet transforms. The first idea of wavelets with IIR filter banks was presented in 1993 by Herley, et al. [2]. They show that IIR filters can lead to more general wavelets. They also gave a complete constructive method, which yields all orthogonal two channel filter banks. where the filter has rational transfer function leading to orthogonal wavelet bases. Half- band Butterworth filters were used to generate those orthonormal wavelets. Since the resulting filter banks were constructed with filters having rational transfer functions, they are realizable. In 2004, Yamashita, et al. [3] proposed an IIR half-band filter with an arbitrary degree of flatness. The application of such filters in filter banks and wavelets was presented. The stability of such filter was guaranteed. Many examples on the designed orthonormal wavelet transform implemented with IIR filter pairs were considered in by Damjanovic, et al. In 2005 [4]. In 2006, low complexity half-band, IIR filters were presented and realized by L. Milic, et al. [5] using two path polyphase structures utilizing allpass filters as components.

In this paper, a new IIR filter bank is used to simulate discrete wavelets transform. The wave digital filter (WDF) is one of the structures of the IIR digital filters [6]. WDFs are known to have many advantageous properties. They have low-coefficient sensitivity with excellent dynamic range leading to implementations with short coefficient word length, and especially, strong stability properties under finite-arithmetic conditions [7], [8]. A class of WDFs that is even more suitable for VLSI implementations is lattice WDFs (LWDFs) [9]. A bi reciprocal LWDF (BLWDF) is a distinctive form of LWDFs [10] that reduces the number of adaptors under certain conditions. In BLWDFs, all the even coefficients are zeros, leaving only the odd-numbered adaptors to be implemented [11]. This reduces the implementation complexity of BLWDFs. It also increases the throughput, compared to the same order LWDFs implementations [9]. So, BLWDFs conducted in this paper, represent the most efficient family of IIR filters and are therefore, of great interest. A linear phase version of those BLWDFs representing a 9<sup>th</sup> order IIR wavelet filter bank is designed using allpass sections. Its multiplier less realization and less-complex FPGA implementation are also presented. The structure of BLWDF is shown in Fig. (1). It consists of two branches, where each branch realizes an Allpass filter. These Allpass filters can be realized using any of the general realization methods, or with regard to some characteristic of the peculiar interest [12].

This paper is divided into five main sections. Besides this introductory section, section II describes the proposed linear phase design method for 9<sup>th</sup> order IIR wavelet filter banks. Matlab programming is used in section III to estimate a suitable coefficient's Wordlength representation. These coefficients are then realized in a multiplier less manner. The implementation results using a Xilinx FPGA device is given in section IV. Finally, section V

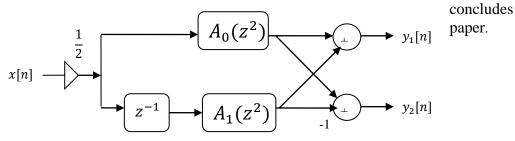


Fig. (1): BLWDF block diagram.



#### II. The Proposed Design

The two-channel allpass-based QMF bank consists of two analysis and two synthesis filters as shown in Fig. (2). Which is realized as a parallel connection of two Allpass filters.

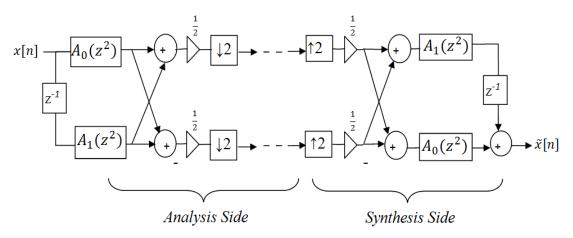


Fig. (2): Two-channel Allpass-based QMF bank.

The  $2N^{th}$  Order real allpass filter has a transfer function G(z), can be expressed as [7]

$$G(z) = \frac{\sum_{n=0}^{N} a_n z^{2(n-N)}}{\sum_{n=0}^{N} a_n z^{-2n}} \dots (1)$$

The related phase function can be expressed as follows:

$$\Phi(\omega) = -2N\omega + 2\arctan\left(\frac{\sum_{n=1}^{N} a_n \sin 2n\omega}{1 + \sum_{n=1}^{N} a_n \cos 2n\omega}\right) \qquad \dots (2)$$

Rearranging Eqn.(2) so that we have the following expression:

$$\frac{\sum_{n=1}^{N} a_n \sin 2n\omega}{1 + \sum_{n=1}^{N} a_n \cos 2n\omega} = \tan\left(\frac{1}{2}(\Phi(\omega) + 2N\omega)\right) \qquad \dots (3)$$

Where  $\Phi(\omega)$  is the desired phase response for the upper or lower branch allpass filter and 2N is the filter order.

Eqn. (3) now defines an approximation problem to determine the coefficients  $\{a_n's\}$  such that function on the left hand side approximates that on the right hand side. Alternatively, if we express the tangent function in terms of sine and cosine functions we have,

$$\frac{\sum_{n=1}^{N} a_n \sin 2n\omega}{1 + \sum_{n=1}^{N} a_n \cos 2n\omega} = \frac{\sin\left(\frac{1}{2}(\Phi(\omega) + 2N\omega)\right)}{\cos\left(\frac{1}{2}(\Phi(\omega) + 2N\omega)\right)} \dots (4)$$

Equating the numerators (or denominators) of Eqn.(4) gives the followings:

$$\sum_{n=1}^{N} a_n \sin 2n\omega = \lambda(\omega) \sin\left(\frac{1}{2}(\Phi(\omega) + 2N\omega)\right) \qquad \dots (5)$$

and

$$\sum_{n=1}^{N} a_n \cos 2n\omega = \lambda(\omega) \cos \left(\frac{1}{2}(\Phi(\omega) + 2N\omega)\right) \qquad \dots (6)$$

Where  $\lambda(\omega)$  Is an arbitrary real function of frequency. To get the desired frequency response,  $\lambda(\omega)$  is chosen as



$$\lambda(\omega) = 0.363 + 0.97765\omega^2 + 0.876\omega^4 \cos(N\omega) \qquad ...(7)$$

Eqn. (5) can be solved to determine the coefficients using the arbitrary real function  $\lambda(\omega)$ given in Eqn. (7).

Using the fact that the functions  $\{\sin(2n\omega)\}, n=1,\ldots,N$ , are an orthogonal set over the range  $[0,\pi]$  as the phase is an odd function, multiplying both sides of Eqn. (5) by  $\sin(2n\omega)$  and integrating over this range give

$$a_n = \frac{2}{\pi} \int_{0}^{\pi} \lambda(\omega) \sin\left(\frac{1}{2}(\Phi(\omega) + 2N\omega)\right) \sin(2n\omega) d\omega \qquad ...(8)$$

For the lower branch, the delay can also be incorporated into the design procedure. The coefficients of the lower branch can be found in a similar way from the following integration:

$$b_n = \frac{2}{\pi} \int_{0}^{\pi} \lambda(\omega) \sin\left(\frac{1}{2}(\Phi(\omega) + 2N\omega + \omega)\right) \sin(2n\omega) d\omega \qquad \dots (9)$$

Where  $\Phi$  ( $\omega$ ) =  $-k\omega$  for  $0 \le \omega \le \frac{\pi}{2}$  and k is the phase slope in the pass band. For a 9<sup>th</sup> order QMF filter, a 4<sup>th</sup> order allpass filter is selected. By applying Eqns. (8) and (9),

the following sets of coefficients can be obtained:

$$a_0 = 1$$
,  $a_1 = 0.3330393784$ ,  $a_2 = 0.0139983361$ .  $b_0 = 1$ ,  $b_1 = 0.36656301954$ ,  $b_2 = 0.01691248172$ .

Substituting these coefficients in Eqn. (1), results in the following allpass function in the upper branch:

$$A_0(z^2) = \frac{z^{-4} + 0.3330393784}{0.0139983361z^{-4} + 0.3330393784z^{-2} + 1} \dots (10)$$

and in lower branch

$$A_1(z^2) = \frac{z^{-4} + 0.36656301954 \ z^{-2} + 0.01691248172}{0.01691248172z^{-4} + 0.36656301954z^{-2} + 1} \qquad \dots (11)$$

For stable and efficient realizations, the structure in Fig. (3) is used with  $A_0(z)$  and  $A_1(z)$ are rewritten in the following equations [13]:

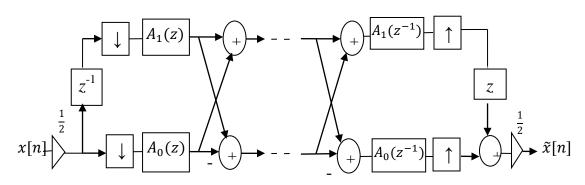


Fig. (3): Computationally efficient realization of the IIR wavelet filter bank.

$$A_0(z) = \frac{z^{-2} + 0.3330393784 \ z^{-1} + 0.0139983361}{0.0139983361z^{-2} + 0.3330393784z^{-1} + 1} \qquad \dots (12)$$



and

$$A_1(z) = \frac{z^{-2} + 0.36656301954 \ z^{-1} + 0.01691248172}{0.01691248172z^{-2} + 0.36656301954z^{-1} + 1} \qquad \dots (13)$$

The above allpass functions  $A_0(z)$  and  $A_1(z)$  can be expressed in the following product forms:

$$A_0(z) = \frac{\alpha + z^{-1}}{1 + \alpha z^{-1}} * \frac{\beta + z^{-1}}{1 + \beta z^{-1}} \dots (14)$$

and

$$A_1(z) = \frac{\sigma + z^{-1}}{1 + \sigma z^{-1}} * \frac{\gamma + z^{-1}}{1 + \gamma z^{-1}} \qquad \dots (15)$$

where the values of  $\alpha$ ,  $\beta$ ,  $\sigma$  and  $\gamma$  are 0.2836967808, 0.0493425976, 0.312431152077 and 0.05413186746, respectively. The frequency response and pole zero plot for the designed lowpass filter are shown in Figs. (4) and (5).

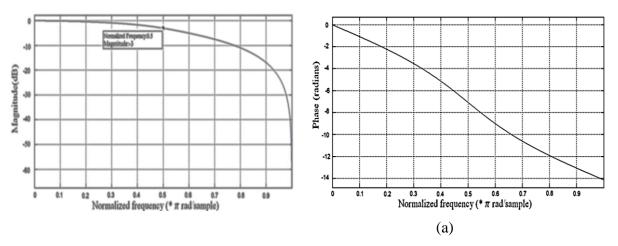


Fig. (4):Frequency response for 9<sup>th</sup> order IIR QMF filter.
(a) Magnitude response (b) Phase response.

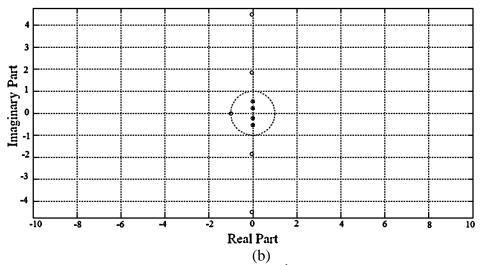


Fig. (5): Pole-zero plot for the designed 9<sup>th</sup> order IIR QMF lowpass filter.



Linear phase response can be presented at filter specification by mean of "Deviation from Linear Phase". It is defined as a distance of each point of a phase response of designed filter from the phase response of ideal filter (straight line) [14]. Figure (6) shows the phase "Deviation from Linear Phase" of a designed filter. The Mean-Square-Error between the two phases can also be used as a measure and it is given by

$$MSE = \frac{1}{L} \sum_{w=0}^{L} \left[ \left| \left( Ph(e^{j\omega}) \right| - \left| Ph_{Linear}(e^{j\omega}) \right| \right]^{2} \dots (16)$$

where  $Ph(e^{j\omega})$  is the designed phase response,  $Ph_{Linear}$  is the phase response of ideal filter (straight line) and L is No. of samples in passband.

The obtained value of *MSE* is 0.076, which is very low indicating the resulting approximate linear phase property of the designed IIR wavelet filter banks.

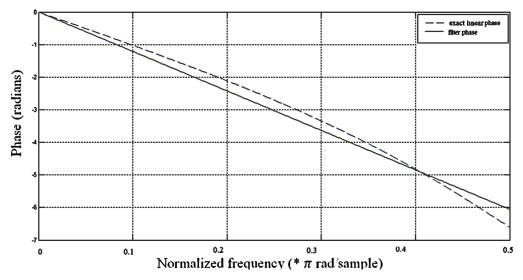


Fig. (6): The phase deviation from linear phase of the designed 9<sup>th</sup> order IIR filter.

#### III. Multiplierless Realization

The low sensitivity characteristic of wave digital filters, allow us to implement the filters coefficients with short wordlengths. In order to select a sufficient wordlength, Matlab environment is used with the application of two gray scale images (Lena and Peppers) as shown in Figs. (7) and (8) to find the minimum wordlength of the BLWDFs coefficients for acceptable PSNR and SNR values (about 30 dB). The correlation coefficient has a close to one-value, and the frequency response of the filter after coefficients quantization closely approximates the frequency response of the original designed filter. This closeness is measured by a maximum deviation in magnitude response  $\Delta Mag_{max}$  and a maximum passband deviation in phase response  $\Delta \varphi_{max}$  (in rads.). A 4-bit wordlength is chosen, which gives the values of the prescribed performance measures illustrated in Table I. These measures show an excellent closeness to the ideal case. The quantized coefficient values are given in Table II. The coefficients in Table II can be implemented in a multiplierless manner after representing them as sum-of-powers-of-two (SPT). Multiplication is then achieved by shift and add.





Original image



Reconstructed image



Approximation



Details

Fig. (7): The analysis and synthesis of Lena image using  $9^{th}$  order IIR QMF.



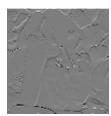
Original image



Reconstructed image



**Approximation** 



Details

Fig. (8): The analysis and synthesis of Peppers image using 9<sup>th</sup> order IIR QMF.

TABLE I
The performance measures of the designed filter after quantization.

performance	Lena	Peppers
measures		
PSNR (dB)	55.2813	46.4135
SNR (dB)	45.8571	40.8264
Correlation	1	0.9997
ΔMag <sub>max</sub>	1.2344*10-4	
$\Delta \phi_{\rm max}$ (in rads.)	4.138*10-4	



TABLE II
The coefficient values of the 9<sup>th</sup> order IIR QMF filter.

Coefficient	Designed coefficient value	4-bit representations
α	0.2836967808	0.3125
β	0.0493425976	0.0625
σ	0.312431152077	0.3125
γ	0.05413186746	0.0625

#### **IV. FPGA Implementation**

The proposed design is described first with VHDL language. Then an FPGA device is used to implement the filter design. It is a 500,000-gate Xilinx Spartan-3E XC3S500E in a 320-ball Fine-Pitch Ball Grid Array package (XC3S500EFG320).

#### A. Implementation of analysis filter bank

An efficient hardware implementation of the BLWDF bank structure (as shown in Fig. (3)) of a 9<sup>th</sup> order discrete wavelet transform can be accomplished using number of processing elements (PEs). Each PE in Fig. (9) is a generic term that refers to a hardware element that executes a stream of instructions. The FPGA device utilization summary for analysis side is illustrated in Table III.

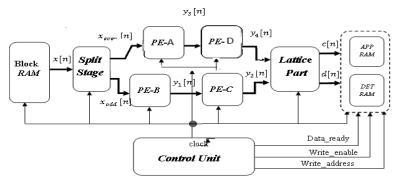


Fig. (9): Structure of wavelet transform analysis side using 9<sup>th</sup> order IIR QMF.

TABLE III
Device utilization summary for analysis side.

Device unitation building for unaryon side.	
	Selected Device: 3s500efg320-4
	Number of Slices: 14 7out of 46563%
	Number of Slice Flip Flops: 133out of 93121%
	Number of 4 input LUTs:214out of 9312 2%
Timing Summary:	
	Speed Grade: -4
Minimum 1	period: 8.984ns (Max. Frequency: 111.309MHz)

#### B. Implementation of synthesis filter bank

The two parallel allpass filters used in this section are  $A_0(z^{-1})$  and  $A_1(z^{-1})$  and are shown in Fig. (10) by the processing elements *PEr-B* and *PEr-A*, respectively. These filters can be implemented as in  $A_0(z)$  and  $A_1(z)$  allpass filters, respectively, by reversing the inputs and

outputs of these filters using last in first out (*LIFO*) register [15] as shown in Fig. (11). This leades to an overall wavelet reconstructed signal with exact linear phase in addition to the appoximate linear phase while decomposing the signal by the wavelet analysis stage. The FPGA device utilization summary for synthesis side is illustrated in Table IV.

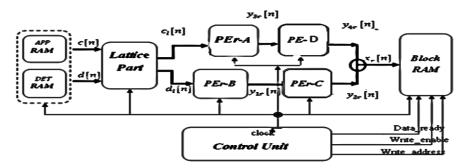


Fig. (10): Structure of wavelet transform synthesis side using 9<sup>th</sup> order IIR QMF.

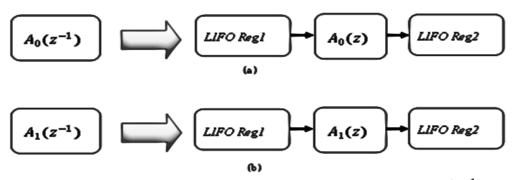


Fig. (11): (a) Implementation of the transfer function  $A_0(z^{-1})$ . (b) Implementation of the transfer function  $A_1(z^{-1})$ 

### TABLE IV Device utilization summary forsynthesis side.

Selected Device: 3s500efg320-4
Number of Slices: 136 out of 46562%
Number of Slice Flip Flops: 141out of 93121%
Number of 4 input LUTs:177out of 9312 2%
Timing Summary:
Speed Grade: -4
Minimum namied, 9 157mg (May, Engguenay, 122 504MHz)
Minimum period: 8.157ns (Max. Frequency: 122.594MHz)

#### v. Conclusions

Approximate linear phase 9<sup>th</sup> order IIR wavelet filter banks utilizing Bireciprocal Lattice Wave Digital Filters (BLWDFs) has been designed and realized by allpass filters. Filter coefficients has been quantized then realized in a multiplierless manner taking into account the low-coefficient sensitivity property of these wave structures. Linear phase IIR wavelet filter bank structures have been obtained and FPGA-implemented with less complexity.

The resulting coefficients can be achieved by shift and add processes only highlighting a multiplierless realization. In addition, a very low phase MSE value (0.076)



indicates the good approximation of linear phase in the analysis side of the proposed wavelet filter banks. In addition, the overall wavelet reconstruction is with linear phase.

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The work was carried out at the college of Engineering. University of Mosul

